UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/670,620	09/25/2003	Jeffrey C. Swanson	10002929-3	6729

7590 03/15/2007

HEWLETT-PACKARD COMPANY
Intellectual Property Administration
P. O. Box 272400
Fort Collins, CO 80527-2400

EXAMINER	
MASKULINSKI, MICHAEL C	
ART UNIT	**PAPER NUMBER**
2113	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
2 MONTHS	03/15/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

UNITED STATES PATENT AND TRADEMARK OFFICE

Commissioner for Patents
United States Patent and Trademark Office
P.O. Box 1450
Alexandria, VA 22313-1450
www.uspto.gov

BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/670,620
Filing Date: September 25, 2003
Appellant(s): SWANSON ET AL.

Michael A. Papalas
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 12, 2006 appealing from the Office action mailed July 14, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings, which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

No amendment after final has been filed.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,867,644	Ranson et al.	2-1999
5,711,240	Tobin et al.	6-1998

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. A nonstatutory obviousness-type double patenting rejection is appropriate where the conflicting claims are not identical, but at least one examined application claim is not patentably distinct from the reference claim(s) because the examined application claim is either anticipated by, or would have been obvious over, the reference claim(s). See, e.g., In re Berg, 140 F.3d 1428, 46 USPQ2d 1226 (Fed. Cir. 1998); In re Goodman, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); In re Longi, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); In re Van Ornum, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); In re Vogel, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and In re Thorington, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) or 1.321(d) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent either is shown to be commonly owned with this application, or claims an invention made as a result of activities undertaken within the scope of a joint research agreement.

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-21 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-17 of U.S. Patent No. 6,662,313 B1. Although the conflicting claims are not identical, they are not patentably distinct from each other because of the following.

Referring to claim 1, claim 1 of U.S. Patent 6,662,313 B1 discloses circuitry for providing external access to signals that are internal to an integrated circuit, said circuitry comprising: a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit; and a trigger event generator receiving a first N bits of sampled data from said network, said trigger event generator including a definable mask and selectively performing a boolean operation on

said sampled data based on said mask to provide a trigger event. Although the conflicting claims are not identical, they are not patentably distinct from each other because claim 1 of U.S. Patent 6,662,313 B1 includes all of the limitations in claim 1 of the instant application. With regard to the additional limitations in claim 1 of U.S. Patent 6,662,313 B1, which are not included in claim 1 of the instant application, the omission of these limitations in claim 1 of the instant application is an obvious expedient since the remaining limitations in claim 1 of U.S. Patent 6,662,313 B1 perform the same function as the limitations in claims 12, 19, and 20 of the instant application (*In re Karlson*, 136 USPQ 184 (CCPA 1963)).

Referring to claim 2, claim 2 of U.S. Patent 6,662,313 B1 discloses wherein said trigger event generator further comprises a switch for selectively providing, as said trigger event, one of (i) a result of said boolean operation on said sampled data, (ii) a performance counter event signal, and (iii) an externally applied trigger signal.

Referring to claim 3, claim 3 of U.S. Patent 6,662,313 B1 discloses a counter providing an intermediate trigger in response to a predetermined number of said trigger events.

Referring to claim 4, claim 4 of U.S. Patent 6,662,313 B1 discloses a trigger delay providing a sample command a predetermined number of cycles following said intermediate trigger.

Referring to claim 5, claim 5 of U.S. Patent 6,662,313 B1 discloses said predetermined number of cycles represent respective operating cycles of the integrated circuit.

Referring to claim 6, claim 6 of U.S. Patent 6,662,313 B1 discloses wherein said predetermined number of cycles represent respective machine clock cycles.

Referring to claim 7, claim 7 of U.S. Patent 6,662,313 B1 discloses a programmable register storing a value corresponding to said predetermined number of cycles.

Referring to claim 8, claim 8 of U.S. Patent 6,662,313 B1 discloses wherein said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles.

Referring to claim 9, claim 9 of U.S. Patent 6,662,313 B1 discloses a sampling circuit responsive to said sample command to identify target data.

Referring to claim 10, claim 10 of U.S. Patent 6,662,313 B1 discloses a trigger delay providing a sample command a predetermined number of cycles following said trigger event.

Referring to claim 11, claim 11 of U.S. Patent 6,662,313 B1 wherein the sampling circuit is responsive to said sample command to identify target data.

Referring to claim 12, claim 1 of U.S. Patent 6,662,313 B1 discloses a sampling circuit responsive to said trigger event to identify target data.

Referring to claim 13, claim 12 of U.S. Patent 6,662,313 B1 discloses said target data comprises said first N bits of sampled data supplied by said network.

Referring to claim 14, claim 13 of U.S. Patent 6,662,313 B1 discloses wherein said target data consists of a second N bits of sampled data supplied by said network.

Referring to claim 15, claims 1 and 14 of U.S. Patent 6,662,313 B1 discloses a FIFO storage array (a memory) that stores at least a portion of the sampled data wherein said sampling circuit includes the FIFO array and the portion of the sampled data is said target data.

Referring to claim 16, claim 15 of U.S. Patent 6,662,313 B1 wherein said sampling circuit includes switching circuitry configured to selectively provide a predetermined portion of said target data.

Referring to claim 17, claim 16 of U.S. Patent 6,662,313 B1 discloses wherein said predetermined portion of said target data is N/M bits wide where N/M is a positive integer.

Referring to claim 18, claim 17 of U.S. Patent 6,662,313 B1 discloses wherein said sampling circuit includes multiplexing circuitry configured to combine M of said portions of said target data into a data unit N bits wide.

Referring to claim 19, claim 1 of U.S. Patent 6,662,313 B1 discloses wherein said sampling circuit includes the FIFO storage array.

Referring to claim 20, claim 1 of U.S. Patent 6,662,313 B1 discloses the FIFO storage that is N/M bits wide where N/M is a positive integer.

Referring to claim 21, claim 1 of U.S. Patent 6,662,313 B1 discloses a FIFO storage array that stores at least a portion of the sampled data.

Claims 1-3, 12-16, and 19 are rejected under 35 U.S.C. 102(b) as being anticipated by Ranson et al., U.S. Patent 5,867,644.

Referring to claim 1:

a. In column 28, lines 57-64, Ranson et al. disclose that various 16:1 multiplexers are physically located at various remote locations around the microprocessor. Each has its inputs coupled to a set of test nodes (a network comprising a plurality of multiplexers physically distributed throughout the integrated circuit, each of said multiplexers having its inputs coupled to a nearby set of nodes within the integrated circuit).

b. In column 15, lines 44-67 continued in column 16, lines 1-5, Ranson et al. disclose that the four bits of present state bus are provided to one of the inputs of comparator so that they may be compared with the contents of storage element, which specifies the present state during which entry will become active (a trigger event generator receiving a first N bits of sampled data from said network). The four bits that are output from the comparator are ANDed together at AND gate, yielding a one-bit match result for present state. Similarly, the contents of storage element 1202 are compared with the eleven bits of state machine input bus by the comparator. An OR gate is used to mask the output bits of the comparator with the contents of the storage element. The results of this masking operation are ANDed together, resulting in a match result for the state machine input bus (said trigger event generator including a definable mask and selectively performing a Boolean operation on said sampled data based on said mask to provide a trigger event).

c. In Figure 4 and in column 13, lines 38-67 continued in column 14, lines 1-62, Ranson et al. teach a FIFO storage array that stores at least a portion of the sampled data.

Referring to claim 2:

a. In column 15, lines 44-57, Ranson et al. disclose the four bits that are output from the comparator are ANDed together at AND gate, yielding a one-bit match result for present state (a result of said Boolean operation on said sampled data).

b. In column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a performance counter event signal).

c. In the Abstract, Ranson et al. disclose that the output devices also include circuitry for generating internal and external triggers (an externally applied trigger signal).

Referring to claim 3, in column 3, lines 55-58, Ranson et al. disclose that the outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times (a counter providing an intermediate trigger in response to a predetermined number of said trigger events).

Referring to claim 12, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors

the external pulse signal (a sampling circuit responsive to said trigger command to identify target data).

Referring to claims 13 and 14, in columns 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted. Specifically in column 23, lines 60-67, Ranson et al. disclose storing only certain data matches (a first and second N bits of sampled data supplied by said network).

Referring to claim 15, in Figure 4, Ranson et al. disclose remote registers for storing the data (said sampling circuit includes a memory storing said target data).

Referring to claim 16, in column 11, lines 16-26, Ranson et al. disclose sample-on-the-fly circuitry that latches the state of the test nodes 0-n whenever a control signal is asserted (switching circuitry configured to selectively provide a predetermined portion of said target data).

Referring to claim 19, in Figure 4, Ranson et al. disclose a storage array in which the bits are shifted serially through the remote registers (wherein said sampling circuit includes a FIFO storage array).

Claims 4-11 are rejected under 35 U.S.C. 103(a) as being unpatentable over Ranson et al., U.S. Patent 5,867,644 as applied to claim 1 above, and further in view of Tobin et al., U.S. Patent 5,771,240.

Referring to claims 4 and 10, in column 3, lines 55-58, Ranson et al. teach an intermediate trigger signal. However, Ranson et al. don't explicitly disclose a trigger delay providing a sample command a predetermined number of cycles following said

intermediate trigger. In column 4, lines 16-31, Tobin et al. disclose a programmable countdown timer that is configured to keep track of the number of clock cycles which pass once its input trigger capture signal is received, and produces a countdown timer enable signal when the number of clock cycles which have passed equals the programmed clock cycle count. It would have been obvious to one of ordinary skill at the time of the invention to include the countdown timer of Tobin et al. into the system of Ranson et al. A person of ordinary skill in the art would have been motivated to make the modification because *the ability of the debug trigger apparatus to precisely control the signaling delay of the trigger capture signal is critical to allowing the test system to iteratively retrieve continuous yet discrete test node signal events from the integrated circuit in order to form a useful trace of events for use in debugging problems and failures of the integrated circuit* (see Tobin et al.: column 4, lines 25-31).

Referring to claim 5, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective operating cycles of the integrated circuit).

Referring to claim 6, in column 4, lines 16-18, Tobin et al. disclose the programmable countdown timer may be set to countdown a programmed number of clock cycles before signaling a trigger capture signal (said predetermined number of cycles represent respective machine clock cycles).

Referring to claim 7, in Figure 8, Tobin et al. disclose a register for the countdown timer (a programmable register storing a value corresponding to said predetermined number of cycles).

Referring to claim 8, in column 3, lines 47-58, Tobin et al. disclose that when an external pulse signal is received, the diagnostics retrieval system may then reset the integrated circuit, reprogram the trigger condition, and set the programmed delay to a second delay value which is a known increment greater than the first delay value (said programmable register selectively increments said value corresponding to said predetermined number of cycles by a predetermined number of said cycles).

Referring to claim 9, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

Referring to claim 11, in column 3, lines 47-49, Ranson et al. disclose a diagnostics retrieval system that initiates operation of the integrated circuit and monitors the external pulse signal (a sampling circuit responsive to said sample command to identify target data).

(10) Response to Argument

On page 5, with respect to claims 1, 2, 12, 15, 16, and 19, the Appellant argues that Ranson et al. don't disclose a FIFO. The Examiner respectfully disagrees. By definition FIFO is a technique for managing a set of items to which additions and deletions are to be made; items are appended to one end of a list and retrieved from the

other end.[1] Thus it must follow that a FIFO storage array is a storage array that uses this technique. In Figure 4, Ranson et al. disclose a staging register 338 and a series of remote registers 344, 346, 348, 350, 352, 354 connected serially. In Figure 5, Ranson et al. disclose the staging register circuitry. It consists of a header generation register 504 and a staging register 500. Both of these registers are FIFO registers because the bits come in at the top at LOAD/SHIFT and then are shifted serially to the last cell in the register at the bottom and are outputted. Further, in Figure 4, Ranson et al. disclose that the data is serially shifted through the remote registers after leaving the staging register. This is also taught in column 13, lines 57-66 continued in column 14, lines 1-12. The remote registers receive the header data first via multiplexer 506 and then the staging register data second via multiplexer 506. The data is shifted serially through the remote registers in a FIFO manner. Therefore, it is the remote registers that are the FIFO storage array.

Further, on page 6, with respect to claims 1, 2, 12, 15, 16, and 19, the Appellant argues, "The Examiner's assertion that the process described above teaches shifting in a FIFO manner is incorrect for at least two reasons. First, as described above, FIFO means "First-In-First-Out," which does not necessarily flow from the cited passage. Specifically, it appears that staging register 500 is loaded before header generation register 504 is loaded, while the contents of header generation register 504 are shifted out before the contents of staging register 500 are shifted out. This does not teach shifting "in a FIFO manner," as asserted by the Examiner." The Examiner respectfully

[1] First-in, first-out definition found in IEEE The Authoritative Dictionary of IEEE Standards Terms, Seventh

disagrees. The Appellant has not pointed to anywhere in the reference of Ranson et al. where this is taught, but rather has made an assumption that the staging register is loaded first and then the header generation register is loaded. Further, the Examiner does not fully understand why the Appellant is concerned over the header data and the header generation register. Claim 1 clearly states storing a portion of the sampled data. The sampled data would have to be the data taken from the chip and this would make up the load or data that follows the header. As stated by the Appellant this data is stored in the staging register and as clarified by the Examiner, the staging register is a FIFO.

Second, it appears the Examiner is assuming that the data and header are loaded into and shifted out of the same register, and that the header is loaded into the one register first and is followed by the loading of the data. However, as shown above, the data and header are loaded into different registers in a different order from that described by the Examiner. Thus, the Examiner's assumption does not hold. Accordingly, the cited portions of Ranson do not teach the above-recited feature of claim 1. Since the cited portions of Ranson do not teach a FIFO storage array, the rejection must fail." The Examiner respectfully disagrees. Although, the header and the data are loaded in different registers, they are shifted in a FIFO manner into the remote registers with the header first and then the data. Further, as pointed out above, both the staging register and the header generation register are FIFO registers and since the claim language only states *a FIFO storage array that stores at least a* ***portion*** *of the*

Edition.

sampled data, the staging register stores a portion of the data and the header generation register stores a portion of the data. For at least the reasons above, Ranson et al. explicitly teach a FIFO storage array that stores at least a portion of the sampled data.

On pages 6-7, with reference to claim 3, the Appellant argues, "However, the cited passage does not teach taking an action in response to a predetermined number of trigger events, much less providing an intermediate trigger in response to a predetermined number of trigger events, much less providing an intermediate trigger in response to a predetermined number of trigger events. In fact, the cited portion does not mention counting trigger events at all." The Examiner respectfully disagrees. In column 3, lines 52-58, Ranson et al. disclose that the output devices coupled to the state machine output bus include counters that are capable of keeping a tally of the number of times a certain user-defined event has occurred. The outputs from the counters may also be used as state machine inputs, so that one event may be defined as a function of a different event having occurred a certain number of times. The user-defined event is the equivalent of a trigger event. All trigger events have to be defined by a user at one point. So as shown above, Ranson et al. disclose counting the number of user-defined (trigger) events and Ranson et al. disclose an intermediate trigger since there are events (trigger events) defined as a function of the counters counting a number of user-defined (trigger) events.

On page 7, with respect to claims 13 and 14, the Appellant argues, "The cited portion of Ranson does not teach these features of claims 13 and 14 at least because it

does not appear to teach that target data comprises or consists of bits of sampled data. Note that claim 1, from which claims 13 and 14 depend, recites that the trigger event generator receives sampled data to provide a trigger event. Further, claim 12, from which claims 13 and 14 depend, recites that a sampling circuit is responsive to the trigger event to identify the target data. However, the cited portion of Ranson does not appear to teach a relationship between sampled data and target data wherein the target data comprises or consists of sampled data as recited in claims 13 and 14." The Examiner respectfully disagrees. In column 23, lines 60-67, Ranson et al. disclose storing only certain data matches such as data match 1 or 0 or both 1 and 0. These data matches are a result comparator circuitry that compares a user-defined (trigger) event to data taken from the bus (sampled data) (see Ranson et al.: column 23, lines 40-59). Thus, Ranson et al. teach a relationship between sampled data and target data wherein the target data comprises or consists of sampled data.

On pages 7-8, with respect to claims 4-11, the Appellant's argument is unpersuasive because the Examiner has shown above how each and every element of the claims is taught by Ranson et al. and Tobin et al.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Michael Maskulinski

Conferees:

Scott Baderman

Robert Beausoliel